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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,540	03/10/2004	Sergey Savastiouk	M-15302-1P US	6386

32605 7590 09/27/2006

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EXAMINER	
LEE, KYOUNG	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 09/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,540	SAVASTIOUK ET AL.	
	Examiner	Art Unit	
	Kyoung Lee	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *47-53 and 55-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *47-53 and 55-76* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 47-49, 52-53, 55-57, 60-63, 70-71, and 73-76 are rejected under 35 U.S.C. 102(b) as being anticipated by Gaynes et al. (U.S. Patent No. 6,165,885).

[Re claim 49] DeFelice discloses the method comprising: forming one or more conductive contact pads (1503) in a first substrate at a top surface of the first substrate (1501); forming dielectric over the one or more contact pads (1513) with the dielectric having one or more openings which overlie the contact pads and also overlie one or more regions adjacent to the contact pads; placing solder paste (1507) into the one or more openings; heating the solder paste to melt the solder (see figures 76-77 and column 44, lines 30-61); [Re claim 47] wherein the region adjacent to the contact pads are less solder wettable than the contact pads; [Re claim 48] wherein the regions adjacent to the contact pads are dielectric regions; [Re claim 52] wherein the first substrate is a semiconductor integrated circuit; [Re claim 53] wherein the first substrate is an integrated circuit packaging substrate which does not include a semiconductor substrate; and [Re claim 62] wherein the solder paste is placed into the openings to fill the one or more openings (see figures 76-77 and column 44, lines 30-48).

[Re claim 57] DeFelice discloses the method comprising: forming one or more conductive contact pads (1503) in a first substrate at a top surface of the first substrate (1501), the one or more conductive contact pads including a first contact pad; forming dielectric (1513) over the one or more contact pads, with the dielectric having one or more openings, the one or more openings comprising a first openings, wherein each of the contact pads occupies at least a portion era bottom surface of at least one of the openings, wherein the first contact pad occupies a first portion of the bottom surface of the first opening but does not occupy a second portion of the bottom surface of the first opening; placing solder paste (1507) into the one or more openings; and heating the solder paste to melt the solder (see figures 76-77 and column 44, lines 30-61); [Re claim 55] wherein the second portion is less solder wettable than the first contact pads; [Re claim 56] wherein the second portion is dielectric; [Re claim 60] wherein the first substrate is a semiconductor integrated circuit; [Re claim 61] wherein the first substrate is an integrated circuit packaging substrate which does not include a semiconductor substrate; and [Re claim 63] wherein the solder paste is placed into the openings after the forming of the dielectric over the one or more contact pads (see figures 76-77 and column 44, lines 30-48).

[Re claim 70] DeFelice discloses the method comprising: forming a first substrate comprising one or more conductive contact pads at a top surface of the first substrate; forming dielectric on the first substrate, the dielectric having one or more openings which overlie the contact pads; wherein a top surface of each of the contact pads comprises a first conductive portion and a second conductive portion less solder

wettable than the first conductive portion; and wherein the one or more openings overlie both the first and the second conductive portions of at least one of the contact pads. (see figures 76-77 and column 44, lines 30-61); [Re claim 71] further comprising: placing solder on the first substrate, the solder being located in each of the one or more openings; and heating the solder to melt the solder (see figures 76-77 and column 44, lines 30-61) [Re claim 73] wherein said solder is not placed on the first substrate before the forming of the dielectric on the first substrate; [Re claim 74] wherein the solder is placed on the first substrate after the forming of the dielectric on the first substrate; [Re claim 75] wherein at least one of the first and second substrates is a semiconductor integrated circuit; and [Re claim 76] wherein the first substrate is an integrated circuit packaging substrate which does not include a semiconductor substrate (see figures 76-77 and column 44, lines 30-48).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 50-51, 58-59, 64-69, and 72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaynes et al. (U.S. Patent No. 6,165,885) in view of DeFelice et al. (U.S. Patent No. 6,190,940).

[Re claim 50-51 and 58-59] Gaynes discloses the method as claimed and rejected in claims 47 and 57, but does not disclose the method wherein comprising soldering one or more contact pads of a second substrate to the one or more contact pads of the first substrate with solder obtained from the solder paste; wherein the second substrate is semiconductor integrated circuit. DeFelice discloses the method wherein comprising soldering one or more contact pads (38) of a second substrate (37) to the one or more contact pads (22) of the first substrate (21) with solder obtained from the solder paste (see figures 2-8 and column 5, lines 30-52); wherein the second (37) substrate is semiconductor integrated circuit (see column 6, 24-28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to in the method of Gaynes in order to connect the first contact pads of the first substrate with the contact pads of the second substrate.

[Re claim 64] Gaynes discloses the method comprising: forming a first substrate comprising one or more conductive contact pads at a top surface of the first substrate, the one or more conductive contact pads comprising a first contact pad; forming dielectric on the first substrate, the dielectric having one or more openings, the one or more openings comprising a first opening, wherein each of the contact pads occupies at least a portion of a bottom surface of at least one of the openings, wherein the first contact pad occupies a first portion of the bottom surface of the first opening but does not occupy a second portion of the bottom surface of the first opening; placing solder on the first substrate, the solder being located in each of the one or more openings,

wherein said solder is not placed on the first substrate before the forming of the dielectric on the first substrate (see figures 76-77 and column 44, lines 30-61).

However, Gaynes does not discloses the method wherein melting the solder in the one or more openings to solder one or more contact pads of a second substrate to the one or more contact pads of the first substrate with the solder. DeFelice discloses the method wherein melting the solder in the one or more openings to solder one or more contact pads of a second substrate to the one or more contact pads of the first substrate with the solder (see figures 3-8 and column 5, lines 30-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to in the method of Gaynes in order to connect the first contact pads of the first substrate with the contact pads of the second substrate.

The combined teachings of Gaynes and DeFelice disclose the method as claimed and rejected in claim 64, and Gaynes also discloses [Re claim 65] wherein the solder is placed on the first substrate after the forming of the dielectric on the first substrate; [Re claim 66] wherein placing the solder on the first substrate comprises placing a solder paste containing the solder on the first substrate; [Re claim 67] wherein the second portion is loss solder wettable than the first contact pad; [Re claim 68] wherein the second portion is dielectric; and [Re claim 69] wherein at least one of the first and second substrates is a semiconductor integrated circuit (see figures 76-77 and column 44, lines 30-61).

[Re claim 72] Gaynes discloses the method as claimed and rejected in claims 71, but does not disclose the method wherein soldering one or more contact pads of a

second substrate to the one or more contact pads of the first substrate with the solder. DeFelice discloses the method wherein comprising soldering one or more contact pads (38) of a second substrate (37) to the one or more contact pads (22) of the first substrate (21) with solder obtained from the solder paste (see figures 2-8 and column 5, lines 30-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to in the method of Gaynes in order to connect the first contact pads of the first substrate with the contact pads of the second substrate.

Response to Amendment

By the response of the non-final action mailed on 7/21/2006, the examiner carefully reviewed and withdrawn the non-final action filed on 4/26/2006. Argument is moot.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kyoung Lee whose telephone number is (571) 272-1982. The examiner can normally be reached on M-F 8:30AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KL 9/25/06

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER